Amendments to the Specification:

Please amend the Title on the title page and on page 1 as follows:

[[IPS]] IN PLANE SWITCHING LIQUID CRYSTAL DISPLAYING APPARATUS FOR IMPROVED LUMINANCE

Please add the following paragraph at page 1, between lines 1 and 2:

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application 09-283834, filed October 16, 1997, and from U.S. Application Nos. 10/200,762, filed July 24, 2002 and 09/110,076, filed July 2, 1998, the entire contents of which are incorporated herein by reference.

Please replace the paragraph beginning at page 1, lines 3-11, with the following amended paragraph:

The present invention relates to an IPS (In ~~Plain~~ Plane Switching) liquid crystal displaying apparatus by generating an electric field parallel to an array substrate to drive the liquid crystal. More particularly, the present invention relates to a construction of a highly bright liquid crystal displaying apparatus increased in aperture ratio by reducing influences of the leakage of electric field from a signal line, thereby reducing the light shielding area.

Please insert the following heading at page 1, between lines 11 and 12:

DISCUSSION OF THE BACKGROUND

Please replace the paragraph beginning at page 1, lines 12-22, with the following amended paragraph:

In an active matrix type liquid crystal displaying apparatus, an IPS system where the direction of the electric field to be applied on the liquid crystal is made parallel to the array substrate is mainly used as a method of obtaining a wider viewing angle (for example, see Japanese Unexamined Patent Publication No. 254712/1996). It is reported that this system ~~enables to remove~~ removes almost all of the change in the contrast and the inversion of the gradation level in changing the viewing-angle direction (see, for example, AsiaDisplay, 95, page, 577 to 580 by M. Oh-e, and others).

Please replace the paragraph beginning at page 1, line 23, to page 2, line 17, with the following amended paragraph:

A construction of one pixel of the conventional IPS liquid crystal displaying apparatus is depicted in Figs. 43a and 43b. Fig. 43a is the plain view thereof. Fig. 43b is a sectional view taken along a line A - A of Fig. 43a. Fig. 44 is a circuit diagram showing an equivalent circuit of one pixel of the pixel electrode of an IPS liquid crystal displaying apparatus. Fig. 45 is a circuit diagram for illustrating the circuit of the IPS liquid crystal displaying apparatus. Referring to Figs. 43a and 43b, reference numeral 1 denotes a glass substrate, numeral 2 denotes a scanning line, numeral 3 denotes a signal line, numeral 4 denotes a thin film transistor (TFT), numeral 5 denotes a driving electrode, numeral 6 denotes an opposite electrode, numeral 7 denotes an electrode for forming the storage capacitance, numeral 8 denotes common line, numeral 9 denotes a gate insulating film, numeral [[10']] 10 denotes a passivation film, numeral 11 denotes a liquid crystal, numeral 12 denotes a BM (black matrix), numeral 14 denotes a contact hole, numeral 15 denotes a source electrode, and

numeral 16 denotes a drain electrode. Numeral 20 denotes an array substrate comprising glass substrate 1, a signal line 3, a driving electrode 5, an opposite electrode 6. Numeral 30 denotes an opposite substrate arranged opposite to the array substrate 20. Numeral 40 denotes a slit which is a gap between the signal line 3 and the opposite electrode 6, and numeral 50 denotes an opening. Referring to Fig. 44 and Fig. 45, the same reference numerals as those of Figs. 43a and 43b depict the same parts or its equivalents as those of Figs. 43a and 43b.

Please replace the paragraph beginning at page 2, line 31, to page 3, line 16, with the following amended paragraph:

This condition is shown by an equivalent circuit in Fig. 44. The TFT 4 is a semiconductor element having three electrodes of a gate electrode, a source electrode 15 and a drain electrode 16. The gate electrode is connected with a scanning line 2 extended from the scanning line driving circuit. The source electrode 15 is connected with the signal line 3 connected with the signal line driving circuit. The remaining drain electrode 16, connected with the driving electrode 5, drives the liquid crystal by an electric field caused between the driving electrode 5 and the opposite electrode 6. Numeral [[13]] 7 denotes a storage ~~capacitance~~ capacitor for storing the electric charge between the driving electrode 5 and the opposite electrode 6. The construction of one pixel will be described in accordance with Fig. 43a and Fig. 43b. In a pixel formed through the crossing between the scanning line 2 and the signal line 3 are provided a driving electrode 5 for driving the liquid crystal layer, an opposite electrode 6 and a TFT 4. In the TFT 4 there are three electrodes. The scanning line 2 connected with the scanning line driving circuit shown in Fig. 4 5 is connected with the gate

electrode of the TFT 4, so as to apply the scanning signal, the scanning line driving circuit outputs, upon the gate electrode of the TFT 4.

Please replace the paragraph beginning at page 3, line 28, to page 4, line 9, with the following amended paragraph:

The sectional construction of the picture section will be described in accordance with Fig. 43b. A driving electrode 5 and an opposite electrode 6 are respectively formed on the glass substrate 1. Although not shown in Fig. 43b, the scanning line 2 and the common line 8 are also formed in the same layer as that of the driving electrode 5 and the opposite electrode 6. The gate insulating film 9 is laminated on a glass substrate by covering the driving electrode, the opposite electrode, the scanning line and the common line, and the signal line 3 is formed on the gate insulating film 9. Although not shown in Fig. 43b, the storage ~~capacitance~~ capacitor forming electrode 7 is also formed in the same layer as that of the signal line 3. A passivation film [[10']] 10 is laminated further on the signal line 3, so as to form the TFT array substrate 20. The TFT array substrate 20 and the opposite substrate 30 is superposed. The IPS liquid crystal displaying apparatus is made with a liquid crystal 11 being sealed between the TFT array substrate 20 and the opposite substrate 30.

Please replace the paragraph beginning at page 4, lines 10-20, with the following amended paragraph:

The IPS liquid crystal displaying apparatus is a system where the electric ~~filed~~ field is caused along the surface of the TFT array substrate 20 between the driving electrode 5 and the opposite electrode 6 provided on the TFT array substrate 20. Thus, the opposite substrate 30 is a no-electrode substrate having no electrode. On the opposite substrate 30 there is

provided a BM 12 which is a light shielding film. Although not shown, the light leaked from a slit 40 of Fig. 43a is to be shielded with a back light, provided on the under side of the TFT array substrate, as a light source in Fig. 43b.

Please replace the paragraph beginning at page 7, line 19, to page 8, line 6, with the following amended paragraph:

In order to prevent such longitudinal crosstalk from being caused, the leaking light transmitting through the slit 40 between the signal line 3 and the opposite electrode 6 is required to be shielded by the BM 12 formed on the opposite substrate 30 and to prevent the electric field, caused between the signal line 3 and the opposite electrode 6, from being interfered with the electric field between the driving electrode 5 and the opposite electrode 6 with the driving electrode 5 and the opposite electrode 6 spaced apart from the opposite electrode 6 of the side end portion on the side of the opening 50, and the signal line 3. When the driving electrode 5 and the opposite electrode 6 are separated from the signal line 3 to make larger the width of the opposite electrode 6 adjacent to the signal line 3, and the aperture ratio of the opening 50, namely, a portion to be occupied by an area where the area of the driving electrode 5 and the opposite electrode 6 and so on is subtracted from the area of the opening 50 with respect to the area of the opening 50 surrounded with broken lines in Fig. 43a, becomes smaller to make the picture quality worse. In order to develop the high picture quality liquid crystal displaying apparatus, it is necessary to ~~shieled~~ shield the light, without reducing the aperture ratio, the electric field to be caused between the signal line 3 and the opposite electrode 6 adjacent to the signal line 3.

Please replace the paragraph beginning at page 8, lines 7-18, with the following amended paragraph:

As clear from Fig. 43b, level of the surface of the passivation film [[10']] 10 which is an upper layer film of the array substrate 20 is not flat (level difference), and the gap between the surface of the passivation film [[10']] 10 and the opposite substrate 30 is not flat. Thus, uneven luminance is likely to be caused, causing the picture quality ~~worse~~ to worsen. The level difference provided makes not only the array substrate inferior due to crack, but also disconnects the wiring on the array substrate due to the level difference portion in the manufacturing operation with a problem in improving the yield factor and reliability of the product.

Please insert the following heading at page 8, between lines 32 and 33:

SUMMARY OF THE INVENTION

Please replace the paragraph beginning at page 8, line 33, to page 9, line 7, with the following amended paragraph:

The first object of the present invention is to solve the problems mentioned above, and to provide an IPS liquid crystal displaying apparatus causing electric field parallel to a glass substrate, the IPS liquid crystal displaying apparatus capable of improving shielding effect against electric field leaking from the signal line, making the opening wide (that is, making opening ratio high) by lowering the light shielding area. Further, the second object of the present invention is to provide a high quality IPS liquid crystal displaying apparatus in which cost for producing the ~~appartur~~ apparatus is decreased by preventing the lines from disconnection thereby improving the yield factor.

Please delete the heading at page 9, line 10, in its entirety.

Please replace the paragraph beginning at page 9, lines 19-38, with the following amended paragraph:

wherein the TFT array substrate is composed of a glass substrate, a gate insulating film formed on the glass substrate, a ~~possivation~~ passivation film formed on the gate insulating film, a plurality of scanning lines for transmitting a scanning signal, the plurality of scanning lines being formed on the glass substrate, a plurality of signal lines for transmitting an image signal, the plurality of signal lines being formed on the gate insulating film, a plurality of pixels arranged in grid like pattern by crossing the plurality of scanning lines with the plurality of signal lines, a plurality of TFTs implementing switching operation of the image signal on the basis of the scanning signals, a plurality of driving electrodes connected with the TFT, a plurality of opposite electrodes arranged in such a manner that each of the plurality of opposite electrodes is opposed to each of the driving electrodes, and a plurality of common lines for mutually connecting each of the opposite electrode of one of the plurality of pixels with the other one of the plurality of pixels,

Please replace the paragraph beginning at page 17, lines 2-9, with the following amended paragraph:

In step 3 (Figs. 6a and 6b) there is ~~formeds~~ formed a signal line 3 simultaneously with a source electrode 15 and a drain electrode 16 of the TFT 4. The signal line 3 functions as a source electrode 15. The signal line 3 is formed of any one of Cr, Al, Mo, Ta, Cu, Al- Cu, Al-Si-Cu, Ti, W or alloy mainly made of them, or alloy made chiefly of them, or a transparent material of such as ITO or the like or their laminated construction.

Please replace the paragraph beginning at page 19, line 6-19, with the following amended paragraph:

The TFT array substrate shown in Figs. 14a, 14b, 15a, 15b, 16a, 16b, 17a, 17b, 18a and 18b includes a pixel of the IPS liquid crystal displaying apparatus shown in Fig. 3, and is formed much more in branch layer than the TFT array substrate shown in Fig. 5. This is due to the difference of a producing step (Figs. 15a and 15b) of forming a scanning line 2, then ~~the continuously~~ successively depositing the gate insulating film 9, the amorphous silicon 9b, and the channel passivation film to cover the scanning line 2, then forming the channel passivation film 21, ion-injecting the impurities such as P and so on into the amorphous silicon with the channel passivation film 21 as a mask to form an n-layer, and forming the channel passivation film transistor.